UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,735	05/25/2004	Chih-Chiang Wen	MTKP0165USA	3734

27765 7590 02/23/2010

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
PORTKA, GARY J	

ART UNIT	PAPER NUMBER
2187	

NOTIFICATION DATE	DELIVERY MODE
02/23/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com.tw

Office Action Summary	Application No.	Applicant(s)	
	10/709,735	WEN ET AL.	
	Examiner	Art Unit	
	GARY PORTKA	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7,8,10-12,14-16,18-23,25-28,30-35 and 38-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,8,10-12,14-16,18-23,25-28,30-35 and 38-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 11, 16, 21 and 25-27 were amended, and claims 38-47 were added by Applicant. Claims 1-4, 7-8, 10-12, 14-16, 18-23, 25-28, 30-35 and 38-47 are pending.

Response to Arguments

2. Applicant's arguments have been considered but are not persuasive. Applicants have argued that none of the references disclose that the processor is inactive while, or is activated after, the electronic device is initialized. Examiner disagrees to the extent understood (see 35 USC 112 rejection below). Hu shows an initialization (activation) of the processor that occurs after the updated firmware is received (Fig. 6), and because the related sections of disclosure describe a queued status (which means the processor is waiting, or idle) the processor is inactive while the device is initializing.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-4, 7-8, 10-12, 14-16, 18-23, 25-28, 30-35 and 38-47 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1, 11, 16, 21, 25, 27 each recite operational firmware that is loaded into a volatile memory, which is not clear because in the described embodiment it does not appear to be firmware as known in the art. This rejection was previously made and the response was that references also included descriptions of firmware downloaded into volatile memory, and that an artisan would have understood it. Examiner disagrees, because in

this case it is not apparent that the recited firmware was ever stored in a ROM type memory as required by definition. Paragraph [0032] of the specification clarifies that the "firmware" may have originated from a host hard drive, then is stored into the device RAM. It is not clear to the Examiner that an artisan would consider that firmware; instead, it appears to simply be “software”. Thus it is not clear what exactly is required to differentiate the recited “firmware” from any software code.

5. Claims 1, 11, 16, 21, 25, 27, 38 and 44 recite some variation of the microprocessor of the electronic device being ‘inactive while’ or ‘initialized after’ the electronic device is initialized. However, this is not understood. Since the microprocessor is a part of the electronic device, it appears that its initialization is a part of the initialization of the device. Put another way, it appears that the microprocessor must at some time be active for the electronic device to completely initialize.

6. The remaining claims are rejected based upon their dependence upon the above the claims.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 2, 7, 8, 10-12, 14, 15, 16, 18-23, 25-28, 30-35, 38-47 are rejected under 35 U.S.C. 103(e) as being obvious over Lewis et al., US 2003/0097552 A1 (hereinafter “Lewis”) and Hu, US 6,170,043 B1 (hereinafter “Hu”).

9. As to claims 1, 7, 11, 15, 16, 20, 21, 25, 27, 30, 38, 44, Lewis discloses a circuit (Fig. 1), download mode, computer system, and controller comprising bus interface (at 106) for communications with a host (management device, 0010), an interface unit electrically coupled to the bus interface for downloading operational firmware from the host (connections between 106 and 112), a control circuit (including 110, 114, 116, and their connections) electrically coupled to the interface unit for transferring the downloaded operation firmware to a volatile memory (112), microprocessor (108) electrically coupled to the control circuit for executing the downloaded operational firmware while stored in the volatile memory, wherein the microprocessor controls the normal operations of the device circuit according to the downloaded firmware (see Abstract, 0010, 0027, 0038). Lewis also discloses receiving initialization data from the host (0030, 0031, 0039, “boot PROM routines"). The download of the operational firmware can be considered in the recited startup procedure to the extent claimed.

10. Lewis does not specifically disclose that the initialization data is received in the startup procedure, nor that the microprocessor is inactive while, or activated after, the device is initialized. However, Hu discloses an analogous non-volatile memory system wherein initialization data is received in a startup procedure, and in which a microprocessor is inactive while, or activated after the device is initialized. See Fig. 6, where Initialize 310, equal to activate, is implemented after the device is initialized with updated firmware via the loop at 322. Clearly a processor may be activated, then considered activated again with the new program. Also, see col. 4 lines 48-51 and col. 5 lines 56-58, where the processor is placed in a "queue status" or simply "waits", both

of which equal being inactive while the device is initialized. The activating of the processor after initialization of the device clearly provides the ability to immediately implement the updated firmware, and thus would have been advantageous to implement in the system of Lewis. Thus it would have been obvious to include the receiving of the initialization date in the startup procedure, and to have the microprocessor is inactive while, or activated after, the device is initialized, because it was taught that the firmware could advantageously be updated and implemented immediately by allowing the processor to activate after the update.

11. Hu further discloses the circuit of claim 1 wherein the bus interface conforms to USB, IDE, SATA, SAS, or SCSI interface standards (Fig. 2, col. 2 lines 59-65, col. 3 lines 45-46). These would have been obvious to an artisan to add to the Lewis-Hu system discussed above to provide compatibility with systems using these standards.

12. As per claims 8, 31, 34, 35, 41, 45, in the Lewis-Hu combination described above, Hu further discloses the circuit of claim 1 wherein the microprocessor executes the downloaded operational firmware without accessing a non-volatile memory, accessing volatile memory (Fig. 2, 212 and 202, col. 3 lines 48-57, col. 4 lines 8-19, col. 6 lines 17-28). This would have been obvious to an artisan to add to the Lewis system discussed above to avoid or reduce the need for the expense of non-volatile memory, and/or its reduced performance versus RAM.

13. As to claims 10, 26, 42, 43, 46, 47, in the Lewis-Hu combination described above, Lewis further discloses the circuit of claim 1 wherein the volatile memory

comprises the downloaded operational firmware being executed by/activating the microprocessor to control normal operations of the circuit (0010).

14. As to claims 12 and 22, Hu further discloses the circuit of claim 1 wherein the normal operations of the circuit at least include reading data from an optical disc (col. 3 lines 62-66), and controlling its rotation. This would have been obvious to an artisan to add to the Lewis system discussed above to use these firmware update circuits for an optical disk drive.

15. As to claim 19, the disclosure of Hu discussed above includes the method of claim 16 further comprising the device transmitting an electrical signal to an application program in the host to begin downloading the operational firmware (col. 5 lines 25-29), which would have been obvious to an artisan to add to the Lewis system discussed above to be able to determine whether firmware versions need to be updated.

16. As to claims 32, 33, Hu further discloses the circuit of claim 27 wherein the host system comprises the volatile memory, or shared by the host and the microprocessor (Figure 2, #212 & col. 4 lines 8-19). This would have been obvious to an artisan to add to the Lewis system discussed above to avoid the expense or space limitations of separate volatile memory at the device.

17. Claims 3, 4, 39, 40 are rejected under 35 U.S.C. 103(a) as being obvious over Lewis, in view of Kamihara et al., US PGPub 2002/0169904, herein Kamihara.

18. Lewis does not disclose using macros. However, as per claims 3, 39, Kamihara teaches the use of a circuit like that of claim 1 wherein the interface unit is a macro (Figure 6, #20 & ¶0095).

19. As to claims 4, 40, Kamihara further discloses the circuit of claim 3 wherein the macro comprises handshaking, data reception, and writing received data into the memory functions [¶0095-0097 & ¶0102].

20. Lewis and Kamihara are analogous art because they are from the same field of endeavor: computer system memory management. At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine a macro interface unit, as disclosed by Kamihara, within the system disclosed by the Lewis. The motivation for doing so would have been for the benefit of aiding the implementation of data transfers, as taught by Kamihara in ¶0096.

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J. Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christian Chace can be reached on (571) 272-4190. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Gary J Portka/
Primary Examiner
Art Unit 2187
February 16, 2010